What is claimed is:

1. A semiconductor memory device, comprising:

a memory cell array having a plurality of memory cells, each memory cell is arranged at an intersection between a drain line and a word line; and

a voltage generator having a first generator and a second generator for generating a drain voltage to be applied to the drain line, wherein the first generator applies the drain voltage to the drain line when an enable signal is input, the second generator applies the drain voltage to the drain line regardless of inputting the enable signal.

2. The semiconductor device according to claim 1, wherein a voltage level of the drain voltage applied by the first generator in the voltage generator is temporarily higher than a predetermined voltage level.

3. A semiconductor memory device, comprising:

a memory cell array having a plurality of memory cells, each memory cell is arranged at an intersection between a drain line and a word line; and

a voltage generator which has a voltage generating circuit for generating the drain voltage having a predetermined value by feed backing an output voltage to an input side based on the enable signal, and feedback stop circuit for temporarily stopping the feedback of the output voltage to increase the drain voltage when the enable signal is supplied thereto.

4. A semiconductor memory device, comprising:

a memory cell array having a plurality of memory cells, each memory cell is arranged at an intersection between a drain line and a word line; and

a voltage generator for generating a drain voltage to be applied to the drain line;

and wherein the memory array has switching circuit for subjecting the drain voltage to be applied from the voltage generator to on-off control in response to a selection signal.

5. A semiconductor memory device, comprising:

a plurality of memory cell arrays each of which has a plurality of memory cells, each memory cell is arranged at an intersection between a drain line and a word line; and

a voltage generator for generating a drain voltage to be applied to the drain line;

a voltage generator which is provided for every plurality of memory arrays, and wherein when the memory array is selected, the voltage generator corresponding to the selected memory array generates the drain voltage and applies the drain voltage to the selected memory array.